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May 17, 2002

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Trademarks, Washington, D.C. on 5/17/02

Shaylor E. Dunn

Date of Signature: 5/17/02

Commissioner for Patents
Washington, D.C. 20231

Re: U.S. Patent Application Serial No. 10/088,988 for METHOD AND
DEVICE FOR PROCESSING CONDITIONAL JUMP
INSTRUCTIONS IN A PROCESSOR WITH PIPELINED
ARCHITECTURE
Our File No. 1406/52

Sir:

Please find enclosed in connection with the subject U.S. patent application the
following documents:

1. An Information Disclosure Statement (2 pages);
2. Forms PTO/SB/08A and PTO/SB/08B (in duplicate);
3. Copies of cited references (10 references); and
4. A return-receipt postcard to be returned to us with the U.S. Patent and
Trademark Office filing stamp thereon.



Commissioner for Patents

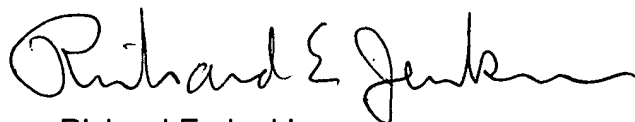
Page 2

May 17, 2002

Although no fee is believed to be due, the Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. 50-0426.

Respectfully submitted,

JENKINS & WILSON, P.A.



Richard E. Jenkins

Registration No. 28,428

Customer No. Bar Code Label:



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PATENT TRADEMARK OFFICE

REJ/sed

Enclosures

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Shaylor E. Dunn

Date of Signature 5/17/02

PATENT



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Xiaoning Nie

Group Art Unit: Not Assigned

Serial No.: 10/088,988

Examiner: Not Assigned

Filed: March 25, 2002

Docket No.: 1406/52

For: METHOD AND DEVICE FOR PROCESSING CONDITIONAL JUMP INSTRUCTIONS IN A PROCESSOR WITH PIPELINED ARCHITECTURE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.56, 1.97, and 1.98, applicants' undersigned attorney brings to the attention of the Patent and Trademark Office the following references. Copies of the references as well as Forms PTO/SB/08A and PTO/SB/08B are attached hereto. This is not to be construed as a representation that a search has been made or that a reference is relevant merely because cited.

U.S. Patent No. 5,928,358 to Takayama et al. discloses an information processing apparatus which accurately predicts whether a branch is taken for a conditional branch instruction, using small-scale hardware.

U.S. Patent No. 5,349,671 to Maeda et al. discloses a microprocessor system generating instruction fetch addresses at high speed.

U.S. Patent No. 5,136,697 to Johnson discloses a system for reducing delay for execution subsequent to correctly predicted branch instruction using fetch information stored with each block of instructions in cache.

French Patent No. 2 770 662 to Eric Bouyoux discloses a microprocesseur pipeline a saut conditionnel en un cycle d'horloge.

German Patent No. DE 38 55 629 T2 to Usami et al. discloses a verzweigungsschaltung für einen Pipeline-Prozessor.

Publication by Mahlke et al. entitled "A Comparison of Full and Partial Predicated Execution Support for ILP Processors", Center for Reliable and High-Performance Computing, pp. 138-149 (June 22, 1995).

Publication by Lee et al. entitled "Pathlength Reduction Features in the PA-RISC Architecture", IEEE, pp. 129-135 (February 24, 1992).

Publication by Mahon et al. entitled "Hewlett-Packard Precision Architecture: The Processor", Hewlett-Packard Journal, pp. 4-21 (August 1986).

Publication by Parker et al. entitled "Control Structure for Making Fast Conditional Branch Decisions", IBM Technical Disclosure Bulletin, Vol. 27, No. 2, pp. 1239-1240 (July 1984).

Publication by Chevillat et al. entitled "Single-Cycle Branch Operations for a High-Speed Microprocessor", IBM Technical Disclosure Bulletin, Vol. 24, No. 4, p. 1951 (September 1981).

Early passage of the subject application to issue is earnestly solicited.

Although no fee is believed to be due, the Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account Number 50-0426.

Respectfully submitted,

JENKINS & WILSON, P.A.

Date: 5-17-02

By:

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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

(use as many sheets as necessary)

Sheet 1 of 1

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| Application Number | 10/088.988 |
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| Filing Date | 03/25/2002 |
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| First Named Inventor | Xiaoning Nie |
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| Art Unit | Not Assigned |
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| Examiner Name | Not Assigned |
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| Attorney Docket Number | 1406/52 |
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Examiner
Signature

Date
Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known

| | |
|------------------------|--------------|
| Application Number | 10/088,988 |
| Filing Date | 03/25/2002 |
| First Named Inventor | Xiaoning Nie |
| Group Art Unit | Not Assigned |
| Examiner Name | Not Assigned |
| Attorney Docket Number | 1406/52 |

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T ² |
|--------------------|-----------------------|---|----------------|
| | B1 | MAHLKE ET AL., "A Comparison of Full and Partial Predicated Execution Support for ILP Processors," Center for Reliable and High-Performance Computing, p. 138-149, (June 22, 1995). | X |
| | B2 | LEE ET AL., "Pathlength Reduction Features in the PA-RISC Architecture," IEEE, p. 129-135, (February 24, 1992). | X |
| | B3 | MAHON ET AL., "Hewlett-Packard Precision Architecture: The Processor," Hewlett-Packard Journal, p. 4-21, (August 1986). | X |
| | B4 | PARKER ET AL., "Control Structure for Making Fast Conditional Branch Decisions," IBM Technical Disclosure Bulletin, p. 1239-1240, (July 1984). | X |
| | B5 | CHEVILLAT ET AL., "Single-Cycle Branch Operations for a High-Speed Microprocessor," IBM Technical Disclosure Bulletin, Vol. 24 (No. 4), p. 1951, (September 1981). | X |
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Examiner
SignatureDate
Considered

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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

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